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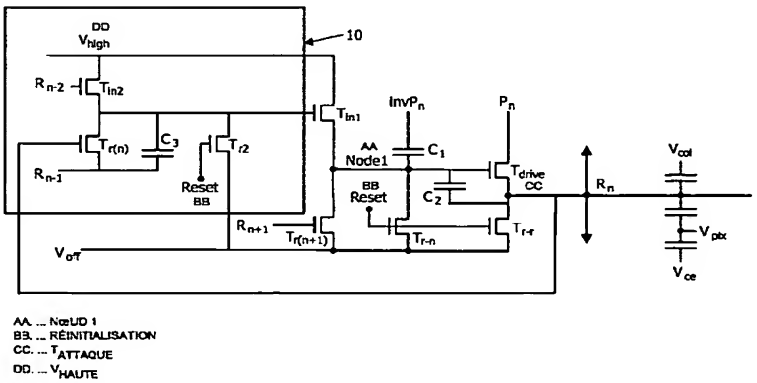
(54) Title: A SHIFT REGISTER CIRCUIT



(57) Abstract: Each stage of a shift register circuit has an input section (60) and an output section (62). The input section of each stage comprises an input section drive transistor (Tdrive) for coupling a first clocked power line voltage (Pn) to the output of the input section (60), an input section compensation capacitor (Ci) for compensating for the effects of a parasitic capacitance of the input section drive transistor (Tdrive) and a first input section bootstrap capacitor (C2) connected between the gate of the drive transistor and the output of the input section. The input section (60) of each stage uses the output (Rn-i) of the input section (60) of at least one preceding stage as a timing control input for controlling a bootstrap function, and the output section (62) of each stage comprises a circuit which receives the outputs of multiple input sections (60) as timing signals for generating output signals for the output loads (64). This circuit uses one stage to provide the required timing signals, and has feedback of timing signals between stages. This stage has low output load, and can therefore be realized with low size components, and the timing signal retain their shape even when there is degradation of the component characteristics. The other stage drives the load, and the output signals are not used as feedback timing signals, so that the output load does not degrade the timing control signals used in other stages.

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